



PTO/SB/17 (05-03)

Approved for use through 04/30/2003. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 2003

Effective 01/01/2003. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$ 320.00

Complete if Known

Application Number	09/904,112
Filing Date	July 11, 2001
First Named Inventor	Chem Basceri
Examiner Name	Jennifer M. Kennedy
Art Unit	2812
Attorney Docket No.	MIO 0057 PA (98-1070)

METHOD OF PAYMENT (check all that apply)☒ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None☐ Deposit Account:Deposit
Account
Number
Deposit
Account
Name

The Director is authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Credit any overpayments☐ Charge any additional fee(s) during the pendency of this application☐ Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account.**FEE CALCULATION****1. BASIC FILING FEE**

Large Entity		Small Entity		Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)		
1001	750	2001	375	Utility filing fee	
1002	330	2002	165	Design filing fee	
1003	520	2003	260	Plant filing fee	
1004	750	2004	375	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	
SUBTOTAL (1)				(\$)	-0-

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra Claims		Fee from below	Fee Paid
Total Claims	<input type="text"/>	-20** =	<input type="text"/>	X <input type="text"/>	= <input type="text"/>
Independent Claims	<input type="text"/>	- 3** =	<input type="text"/>	X <input type="text"/>	= <input type="text"/>
Multiple Dependent				<input type="text"/>	= <input type="text"/>

Large Entity		Small Entity		Fee Description
Fee Code	Fee (\$)	Fee Code	Fee (\$)	
1202	18	2202	9	Claims in excess of 20
1201	84	2201	42	Independent claims in excess of 3
1203	280	2203	140	Multiple dependent claim, if not paid
1204	84	2204	42	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

**or number previously paid, if greater; For Reissues, see above

FEE CALCULATION (continued)**3. ADDITIONAL FEES**

Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for <i>ex parte</i> reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	410	2252	205	Extension for reply within second month	
1253	930	2253	465	Extension for reply within third month	
1254	1,450	2254	725	Extension for reply within fourth month	
1255	1,970	2255	985	Extension for reply within fifth month	
1401	320	2401	160	Notice of Appeal	
1402	320	2402	160	Filing a brief in support of an appeal	320
1403	280	2403	140	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,300	2453	650	Petition to revive - unintentional	
1501	1,300	2501	650	Utility issue fee (or reissue)	
1502	470	2502	235	Design issue fee	
1503	630	2503	315	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	750	2809	375	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	750	2810	375	For each additional invention to be examined (37 CFR 1.129(b))	
1801	750	2801	375	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify)

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$ 320.00

SUBMITTED BY

(Complete if applicable)

Name (Print/Type)	Susan M. Luna	Registration No. (Attorney/Agent)	38,769	Telephone	937-223-2050
Signature	<i>Susan M. Luna</i>	Date	07/22/2003		

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

This collection of information is required by 37 CFR 1.17 and 1.27. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of

Applicants : Basceri et al.
Serial No. : 09/904,112
Filed : July 11, 2001
Title : CAPACITOR WITH HIGH DIELECTRIC CONSTANT MATERIALS
AND METHOD OF MAKING
Docket No. : MIO 0057 PA (98-1070)
Examiner : J. Kennedy
Art Unit : 2812

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on July 22, 2003.

Susan M. Fuma

Agent

Reg. No. 38,769

BRIEF ON APPEAL

This is an appeal from the Office Action mailed May 8, 2003, finally rejecting claims 1-6, 8-12, 15, 22-30, 37-50, 57-63, 74-76 and 100-105 in the application. A Notice of Appeal was timely filed on May 28, 2003, with the accompanying fee. Our check in the amount of \$320.00 accompanies this Brief in accordance with 37 CFR §1.17(c).

Real Party in Interest

The real party in interest in this application is Micron Technology, Inc., by an assignment from the named inventors recorded in the files of the U.S. Patent and Trademark Office at Reel 012234, Frame 0648.

Related Appeals and Interferences

There are no related cases in which an appeal or interference has been filed.

RECEIVED
JUL 29 2003
TECHNICAL STAFF
JUL 29 2003

Status of Claims

Claims 1-72, 74-76 and 80-106 are pending in this application. Claims 7, 13-14, 16-21 31-36, 51-56, 64-72, 80-99, and 106 have been withdrawn from consideration. Claims 73 and 77-79 were previously cancelled. Accordingly, claims 1-6, 8-12, 15, 22-30, 37-50, 57-63, 74-76 and 100-105 are before this Board for consideration on appeal. A copy of the appealed claims is found in the Appendix attached to this brief.

Status of Amendments

All of the amendments previously filed in this application have been entered.

Summary of the Invention

The present invention is directed to a method of making stabilized capacitors and DRAM cells. In one embodiment, the method includes depositing a first layer of high dielectric constant oxide dielectric material such as Ta_2O_5 or $\text{Ba}_x\text{Sr}_{(1-x)}\text{TiO}_3$ onto a conductive oxide electrode which preferably comprises RuO_x or IrO_x , and simultaneously oxidizing the conductive oxide electrode and first layer of high dielectric constant oxide dielectric material. A second layer of the high dielectric constant oxide material is then deposited onto the first layer of the conductive oxide electrode, and an upper layer electrode is deposited onto the second layer of high dielectric constant oxide dielectric material.

As described in the specification at pages 5-7 and illustrated in Fig. 1, the capacitor 22 of the present invention is provided on an insulating layer 16 and electrically conductive plug 20 of a semiconductor bulk silicon substrate 12. The conductive plug 20 constitutes a node to which an electrical connection to the capacitor 22 may be made. As shown, the capacitor 22 comprises an oxide electrode 24 which is deposited onto the insulating layer 16 and conductive plug 20. The oxide electrode 24 is formed by depositing RuO_x or IrO_x using chemical vapor deposition.

A thin layer of a high dielectric constant oxide dielectric material 28 is deposited on oxide electrode 24. The stack, including the layer of oxide dielectric 28, and the oxide electrode 24, is oxidized. The oxidation is preferably carried out by a gas plasma treatment at a temperature of about 400°C . This step provides the surface, and preferably an upper portion of

the oxide electrode, with enough oxygen so that electrode 24 is stable with the oxide dielectric layer 28.

After oxidation, a second layer 30 of high dielectric constant oxide dielectric material is deposited on layer 28. The second layer is preferably oxidized by plasma treatment, furnace oxidation, or rapid thermal oxidation.

A top electrode 32, which preferably comprises RuO_x or IrO_x , is deposited on second layer 30. The top electrode 32 is preferably oxidized, such as by a gas plasma treatment. Alternatively, a permeable electrode 34 (preferably platinum) may be deposited on top layer electrode 32 and annealed under oxidizing conditions which oxidizes the top layer electrode 32.

As illustrated in Fig. 2 and described at pages 9 and 10, when RuO_x is used as oxide electrode 24, an alternative method is to oxidize the upper surface of the RuO_x layer 24 prior to Ta_2O_5 deposition to provide a stable $\text{RuO}_x/\text{Ta}_2\text{O}_5$ interface.

As illustrated in Fig. 3 and described at pages 10-11, a DRAM cell may also be formed in accordance with another embodiment of the present invention which includes a semiconductor substrate 40 including two memory cells having a capacitor 42 and a shared bit contact 44. The capacitors 42 comprise a first capacitor electrode 50, a capacitor dielectric 52 comprising a first layer of a high dielectric constant oxide dielectric 52a, a second layer of a high dielectric constant oxide dielectric material 52b, and a second capacitor electrode/cell plate 54. These layers are formed using the conductive oxide electrode materials and high dielectric constant oxide dielectric materials and methods described above.

The method of the present invention provides an advantage during fabrication in that the oxidation of the first and second oxide dielectric layers occurs at lower temperatures than prior deposition processes (i.e., less than 700°C) because no oxygen is lost through diffusion to the bottom oxide electrode during the gas plasma treatments.

Issues Presented

The issues presented for review on appeal are:

- 1) Whether the Examiner erred in rejecting claims 1-6, 15, 22-30, 37-42, 45-49, 74-76, and 100-105 under 35 U.S.C. 102(e) as being anticipated by Kunitomo et al. (U.S. 6,235,572).

- 2) Whether the Examiner erred in rejecting claims 8-12, 43-44, 50 and 57-61 under 35 U.S.C. 103(a) as being unpatentable over Kunitomo et al. in view of Joo (U.S. 5,879,957).
- 3) Whether the Examiner erred in rejecting claims 11-12 and 62-63 under 35 U.S.C. 103(a) as being unpatentable over Kunitomo et al. and Joo in view of Kingon et al. (U.S. 5,555,486).

Grouping of Claims

The Examiner has made three grounds of rejection, rejecting claims 1-6, 15, 22-30, 37-42, 45-49, 74-76, and 100-105 under 35 U.S.C. 102(e) as being anticipated by Kunitomo et al. (U.S. 6,235,572); rejecting claims 8-12, 43-44, 50 and 57-61 under 35 U.S.C. 103(a) as being unpatentable over Kunitomo et al. in view of Joo (U.S. 5,879,957); and rejecting claims 11-12 and 62-63 under 35 U.S.C. 103(a) as being unpatentable over Kunitomo et al. and Joo in view of Kingon et al. (U.S. 5,555,486).

The application contains eight rejected independent claims, namely, claims 1, 8, 11, 15, 28, 40, 50, and 100. Applicants submit that the claims do not stand or fall together. The patentability of each independent claim will be separately argued. Additionally, the separate patentability of dependent claims 2-4, 6, 22-24, 42, 45, and 47-79 will be argued.

The References

Kunitomo et al., U.S. Patent No. 6,235,572. Kunitomo et al. teach a method of manufacturing a semiconductor device including a capacitor C comprising two or more tantalum oxide films 56 and 58 having a polycrystalline structure, a lower electrode 54 formed of ruthenium, tungsten or titanium, and an upper electrode 62 comprised of titanium nitride. The method includes the steps of forming lower electrode 54 by depositing a ruthenium film 51 and reaction protect layer 53, depositing a first tantalum oxide film 55 on the semiconductor substrate 1, and subjecting the tantalum oxide film to a heat treatment to polycrystallize the film. The heat treatment may be performed in a single step (temperature of 700 to 850°C in an oxygen atmosphere) or in two separate steps (temperature of 600°C or less followed by second treatment at 650 to 850°C in an oxygen atmosphere). A second tantalum oxide film 57 is then deposited

on the first crystallized tantalum oxide film 56 and heat treated to crystallize and form second film 58. Titanium nitride film is deposited on the crystallized tantalum oxide film 58 to form upper electrode 62.

Joo, U.S. Patent No. 5,879,957. Joo teaches a method of making a capacitor for a semiconductor device in which, in one embodiment, an oxide layer 32 is formed on a silicon substrate 31, and a ruthenium layer 35 is formed on a polysilicon plug 34 and oxide layer 32. A conductive ruthenium oxide layer 36 is formed on the ruthenium layer 35 by a reactive sputtering method, a thermal oxidation method, or a plasma oxidation method, and a platinum layer 37 is formed on the Ru oxide layer 36. A dielectric layer 40 is formed over the surface of platinum layer 37 and a second platinum layer 41 is formed on the dielectric layer.

Kington et al., U.S. Patent No. 5,555,486 Kington et al. teach the use of capacitors having hybrid electrode structures. The top electrode comprises a conductive layer 25 which may comprise a hybrid electrode such as Pt/RuO₂ or RuO₂/Pt.

ARGUMENT

I. Summary of Argument

The Examiner has failed to establish, by evidence or reasoning, that claims 1-6, 15, 22-30, 37-42, 45-49, 74-76, and 100-105 are anticipated by Kunitomo et al. Kunitomo et al. do not teach or suggest a method that includes oxidizing a conductive oxide electrode and a first layer of high dielectric constant oxide dielectric material such that the surface of the conductive oxide electrode is provided with enough oxygen to provide stability with the first layer of high dielectric constant oxide dielectric material as claimed.

Nor has the Examiner established a prima facie case, by evidence or reasoning, that any of the rejected claims would have been obvious with respect to the proposed combination of references. The Examiner relies on Joo for teaching oxidation of a ruthenium oxide layer, but

ignores the fact that neither Joo nor Kunitomo et al. teach oxidation of an upper layer electrode as claimed.

Nor do the combined teachings of Kunitomo et al., Joo, or Kingon et al. teach or suggest depositing a gas permeable electrode on an upper layer electrode and oxidizing the upper layer electrode through the gas permeable electrode as claimed.

II. Kunitomo et al. do not anticipate claims 1-6, 15, 22-30, 37-42, 45-49, 74-76, and 100-105.

In order for a reference to anticipate claimed subject matter, each and every limitation in the claims must either be explicitly disclosed by, or inherent from, the reference. *Diversitech Corp. v. Century Steps, Inc.*, 7 USPQ2d 1315, 1317 (Fed. Cir. 1988); *Kalman v. Kimberly Clark Corp.*, 218 USPQ 781, 789 (Fed. Cir. 1983). Moreover, it is incumbent upon the Examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference. *Lindemann Maschinenfabrik GmbH v. American Hoist and Derrick*, 221 USPQ 481 (Fed. Cir. 1984); *Ex parte Levy*, 17 USPQ2d 1461 (PTOBPAI 1990). Finally, there must be a disclosure in a single reference of all claim elements arranged as in that claim. *Panduit Corp. v. Dennison Mfg. Co.*, 227 USPQ 337, 350 (Fed. Cir. 1985).

Applicants' claim 1 recites, inter alia, a method of forming a capacitor comprising providing a conductive oxide electrode (lower electrode), depositing a first layer of a high dielectric constant oxide dielectric material on the conductive oxide electrode, and oxidizing the conductive oxide electrode and first layer of high dielectric constant oxide dielectric material under oxidizing conditions such that at least the surface of conductive oxide electrode is provided with enough oxygen to provide stability with the first layer of high dielectric constant oxide dielectric material.

Kunitomo et al. teach lower electrodes (54) which are formed from a reaction protect layer 53 such as a ruthenium oxide film, and a film 51 which may comprise a ruthenium oxide film, tungsten film, or titanium nitride film. In order to anticipate applicants' claim 1, one skilled in the art would have to oxidize the tantalum oxide film 56 and electrodes 54 of Kunitomo et al. in a manner which provides the electrodes 54 with sufficient oxygen to be stable with the high dielectric constant oxide material.

Kunitomo et al. do not teach a method in which the lower electrodes 54 and tantalum oxide layer 56 are oxidized as claimed. Rather, Kunitomo et al. teach **crystallizing** the tantalum oxide layer 56 in an oxidation atmosphere. The Examiner maintains at pages 3 and 4 of the final rejection that Kunitomo teaches that the lower electrodes are oxidized because "Kunitomo teaches that the tantalum oxide, and consequently the lower electrode is subjected to a heat treatment at a temperature of 650°C or more in an oxidation atmosphere." The Examiner further suggests that the conductive oxide layer of Kunitomo "is provided with enough oxygen so as to be stable with the oxide dielectric layer" as a result of such a heat treatment. However, this treatment refers to crystallization of the tantalum oxide, and there is no explicit teaching or suggestion in Kunitomo et al. that the lower electrodes 54 become oxidized due to the tantalum oxide layer 55 being crystallized. Nor is there any explicit teaching or suggestion in Kunitomo et al. that such a crystallization step would result in a surface of the conductive oxide electrode being provided with enough oxygen to provide stability with the layer of high dielectric constant oxide dielectric material. Rather, Kunitomo et al. teach that the oxidation atmosphere is desired "to recover oxygen defect of crystallized tantalum oxide and to attain a polycrystalline tantalum film having excellent crystal characteristics." See col. 18, lines 54-58. Kunitomo is silent with respect to oxidation of lower electrodes 54.

Also at page 4 of the final rejection, the Examiner refers to col. 21, lines 15-34 of Kunitomo et al., asserting that the lower electrodes are oxidized when performing the crystallization process of the tantalum oxide film. Applicants wish to point out that Kunitomo teaches that this occurs only when a ruthenium oxide layer is formed on the electrodes in advance, which requires that one choose ruthenium oxide as the conductive oxide electrode in the first place. And, as previously pointed out, Kunitomo et al. teach various methods of preventing further oxidation of the electrodes 54 and/or the crystallized films 56 and 58. See col. 19, lines 15-25; and col. 21, lines 27-28. One would have to selectively pick and choose from among the many disparate teachings of Kunitomo et al. to arrive at the claimed invention. Claim 1 is clearly patentable over Kunitomo et al.

Furthermore, Kunitomo et al. do not teach or suggest oxidation of both the lower electrode and dielectric material by a gas plasma treatment as recited in dependent claims 2 and

3. Rather, Kunitomo et al. appear to teach away from plasma treatment of tantalum oxide films as they state that tantalum oxide films subjected to plasma treatment have a lower dielectric constant than crystallized tantalum oxide films and are "therefore disadvantageous for high integration of a DRAM." See col. 2, lines 22-27. In order for there to be anticipation, there must be some explicit teaching in Kunitomo et al. to oxidize using a gas plasma.

Nor do Kunitomo et al. teach or suggest a gas plasma treatment at a temperature range of from about 250°C to 500°C as recited in dependent claim 4. Rather, Kunitomo et al. teach heat treatment at a temperature of 650°C or more. See col. 18, lines 46-50. While Kunitomo et al. teach the use of lower oxidation temperatures, i.e., 600°C or less, such lower temperatures are not used in connection with a gas plasma oxidation treatment and are used only when crystallization of the tantalum oxide film is carried out separately from oxidation processing and the lower electrode is **not** oxidized. See col. 19, lines 8-25.

With regard to claim 6 which recites the use of amorphous tantalum oxide, applicants wish to point out that Kunitomo et al. teach only the use of **crystallized** tantalum oxide film. As pointed out above, Kunitomo et al. teach away from the use of amorphous films. See col. 2, lines 22-42. Claim 6 is clearly patentable over Kunitomo et al. For all of these reasons, claims 1-6 and 74-76 are patentable over Kunitomo et al.

Applicants' independent claim 15 further recites a method where the high dielectric constant dielectric material comprises Ta₂O₅, and recites that the second layer of high dielectric constant oxide dielectric material is oxidized. Kunitomo et al. do not teach or suggest oxidizing the second layer of crystalline tantalum oxide, but rather teach that further oxidation is restricted so as to avoid stress on the crystallized tantalum oxide film 58. See col. 21, lines 27-30. Nor do Kunitomo et al. teach or suggest oxidizing the second layer of tantalum oxide by rapid thermal oxidation as recited in claims 22-24. Claims 15 and claims 22-27, which depend therefrom, are patentable over Kunitomo et al.

Independent claim 28 recites the additional steps of oxidizing and crystallizing the second layer of dielectric material, and depositing an upper layer electrode on the second layer of dielectric material. As pointed out above, Kunitomo et al. do not teach or suggest oxidizing their second film layer 58, nor do Kunitomo et al. teach providing the surface area of the conductive oxide electrode with sufficient oxygen to be stable with the first layer of oxide dielectric material

as claimed. Nor do Kunitomo et al. teach rapid thermal oxidation as recited in claims 37-39. Claims 28-30 and 37-39 are patentable over Kunitomo et al.

Claim 40 recites, inter alia, a method of forming a capacitor comprising providing a conductive oxide electrode selected from the group consisting of RuO_x and IrO_x , depositing a first layer of a dielectric material selected from the group consisting of Ta_2O_5 and $\text{Ba}_x\text{Sr}_{(1-x)}\text{TiO}_3$ on the conductive oxide electrode, oxidizing the conductive oxide electrode and first layer of dielectric material with a gas plasma such that at least the surface area of the conductive oxide electrode is provided with enough oxygen to provide stability with the first layer of dielectric material, depositing a second layer of dielectric material on the first layer of dielectric material, depositing an upper layer electrode on the second layer of dielectric material, and oxidizing the upper layer electrode.

As previously pointed out, Kunitomo et al. do not teach oxidizing both the lower electrode 54 and tantalum oxide film 56 by a gas plasma treatment as claimed. Nor do Kunitomo et al. teach or suggest that the surface of the electrode 54 is provided with enough oxygen to provide stability with the first tantalum oxide film layer 56.

Further, as applicants previously pointed out, one skilled in the art would have to pick ruthenium oxide as the lower electrode from among several of Kunitomo's disclosed materials including tungsten, titanium nitride, and ruthenium. See col. 18, lines 15-17. The Examiner maintained in the final rejection that "when a species is clearly named, the species claim is anticipated no matter how many other species are additionally named." The Examiner further asserted that Kunitomo et al. anticipate the claims because they disclose all of the elements of the claimed invention, i.e., a ruthenium oxide lower electrode. However, applicants wish to remind the Examiner that the present claims are directed to a multi-step **method** of forming a capacitor, not to a chemical compound. The Examiner's species/genus logic is limited to composition. Even if one picks and chooses from the materials disclosed in Kunitomo et al. to meet one step in the process, that does not equate to anticipating the entire claim which recites multiple steps.

Accordingly, claim 40 is clearly patentable over Kunitomo et al. Nor do Kunitomo et al. teach a gas plasma oxidation method at the temperature range recited in claim 42. For all of these reasons, claims 40-42 are also patentable over Kunitomo et al.

Dependent claim 45 further recites that the upper layer electrode is selected from RuO_x and IrO_x . Kunitomo et al. teach the use of titanium nitride as the upper layer electrode. While Kunitomo et al. teach that a ruthenium oxide film may be used in place of titanium nitride, one would have to be motivated to pick and choose ruthenium oxide as the upper electrode. This negates anticipation. See *In re Arkley*, 172 USPQ 524 (CCPA 1972).

Dependent claims 47, 48, and 49 recite the steps of oxidizing the surface of the conductive oxide electrode prior to depositing the first layer of dielectric material, where the surface of the conductive oxide electrode is oxidized at a temperature of from about 400 to 475°C in an atmosphere containing a gas selected from O_2 , O_3 , and N_2O . Kunitomo et al. do not teach oxidizing the surface of their lower electrodes prior to depositing the tantalum oxide film. Nor do Kunitomo et al. teach oxidation of their lower electrode at a temperature of 400 to 475°C using a gas as claimed. While Kunitomo et al. teach oxidation processing at 400°C in an ozone atmosphere, such a condition is referred to as a loose condition in which the lower electrode is **not** oxidized. See col. 19, lines 21-26.

Claims 100-105 recite a method of forming a DRAM cell which includes the steps of depositing a first layer of a high dielectric constant oxide dielectric material on a conductive oxide electrode, oxidizing the conductive oxide electrode and first layer of high dielectric constant dielectric material such that the surface area of the conductive oxide electrode is provided with enough oxygen to provide stability with the first layer of high dielectric constant oxide dielectric material, depositing a second layer of high dielectric constant oxide dielectric material on the first layer, depositing an upper layer electrode on the second layer, and providing a field effect transistor for connection with the conductive oxide electrode and bit line. These claims are believed to be patentable for the same reasons discussed above with regard to claims 1-6.

III. The Examiner's burden of establishing a prima facie case of obviousness has not been met.

It is well established that the burden of establishing a prima facie case of obviousness resides with the Examiner. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); *In re Piasecki*, 745 F.2d 1468, 223 USPQ 785 (Fed. Cir. 1984). This burden can be satisfied only by

showing some objective teaching in the prior art, or that knowledge generally available to one of ordinary skill in the art, would lead that individual to the claimed invention. Both the teaching and a reasonable expectation of success must be found in the prior art, not in applicants' disclosure. *In re Vaeck*, 20 USPQ2d 1438 (Fed.Cir. 1991).

Where the teachings of references are proposed to be combined, it is incumbent upon the Examiner to explain why the combination of reference teachings is proper. The suggestion to modify the reference teachings must come from the references themselves, not from applicants' disclosure. See *In re Laskowski*, 871 F.2d 115, 117, 10 USPQ2d 1397, 1398-99 (Fed. Cir. 1989); *In re Fine*, supra 837 F.2d at 1075 ("[T]eachings of references can be combined, only if there is some suggestion or incentive to do so. Here, the prior art contains none."); *Uniroyal v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 1051, 5 USPQ2d 1434 (Fed. Cir.), cert. denied, 109 S. Ct. 75 (1988) ("When prior art references require selective combination...to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gleaned from the invention itself. Something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination.") Applicants submit that the proposed combination of references here are not based on any objective teaching or suggestion in the references themselves, but rather are based on prohibited hindsight using the claimed invention as a blueprint. *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 227 USPQ 543 (Fed. Cir. 1985).

Where no expressed teaching or suggestion is apparent from the references, the Examiner must establish, with evidence or reasoning, why one skilled in the art would have been led by the relevant teachings of the applied references to make the proposed combination. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984); *ACS Hospital System, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 221 USPQ 929 (Fed. Cir. 1984).

Applicants submit that upon close examination, the Examiner did not meet her burden of establishing a prima facie case of obviousness as to any of the claims on appeal.

IV. The combined teachings of Kunitomo et al. and Joo do not render the claims obvious

With regard to the rejection of claims 8-12, 43-44, 50 and 57-61 based on Kunimoto et al. in view of Joo, the Examiner has acknowledged that Kunitomo et al. do not disclose the step of

oxidizing the upper layer electrode using a gas plasma as recited in claims 8-10. The Examiner relies on Joo for teaching a method of oxidizing an upper layer electrode utilizing a gas plasma, referring to col. 4, lines 46-56. However, this teaching refers to the **formation** of the ruthenium oxide layer 36 on the ruthenium layer 35, not **oxidation** of the upper layer electrode as claimed. Further, Joo teaches that the ruthenium oxide layer may be formed by any of a reactive sputtering method, a thermal oxidation method, or a plasma oxidation method. There is no teaching or suggestion in Joo or Kunitomo et al. which would lead one skilled in the art to choose a plasma oxidation method for oxidation of an upper layer electrode as claimed. While the Examiner asserts in the final rejection that one skilled in the art would choose a plasma method rather than a thermal method "so that the thermal budget may be lowered," the Examiner is reminded that Kunitomo et al. teach away from the use of gas plasma. See col. 2, lines 22-27. Nor is there any teaching or suggestion in Joo of performing a plasma oxidation within the claimed temperature range.

Further, as applicants previously pointed out, neither Kunitomo et al. nor Joo teach or suggest oxidizing an **upper** layer electrode. While Joo teaches that a ruthenium oxide layer 36 may be formed by an oxidation method, this layer comprises the **lower** electrode of the capacitor, not an upper layer electrode. See col. 5, lines 27-30. The Examiner has previously responded by stating that she did not rely upon Joo et al. to disclose forming the upper electrode of ruthenium oxide, only to show the method of forming ruthenium oxide. However, Joo's teaching that ruthenium oxide may be **formed** by an oxidation method does not make it obvious to **oxidize an upper layer electrode** as claimed. At best, Joo might suggest forming Kunitomo's lower electrode using such a method. But such would not result in the claimed method. The fact that one skilled in the art *could* perform a step in a process in a certain way does not establish the requisite suggestion or motivation to do so. Claims 8-10 are clearly patentable over the combination of Kunitomo et al. and Joo.

With regard to claims 11-12, which recite depositing a gas permeable electrode (platinum) on the upper layer electrode and oxidizing the upper layer electrode through the gas permeable electrode, applicants wish to point out that neither Kunitomo et al. nor Joo et al. teach or suggest such process steps. The Examiner has provided no substantive reasoning for rejecting these claims. Applicants also wish to point out that the Examiner admitted at page 8 of the final

rejection that Kunitomo et al. and Joo et al. "do not disclose the method of forming a platinum electrode on the upper layer electrode."

With regard to claims 43-44, applicants wish to point out that these claims depend from independent claim 40, which the Examiner did not reject based on the combined teachings of Kunitomo et al. and Joo. Again, neither Kunitomo et al. nor Joo et al. teach oxidizing an upper layer electrode using a gas plasma at the claimed temperature range.

With regard to the rejection of claims 50 and 57-63, independent claim 50 recites the step of oxidizing the upper layer electrode, which step is not taught or suggested by either Kunitomo et al. or Joo as discussed above. Nor do Kunitomo et al. nor Joo teach oxidation of an upper layer electrode using a gas plasma as recited in claims 60-61.

With regard to claims 57-59 which recite oxidation of the second layer of dielectric material by rapid thermal oxidation, applicants submit that neither Kunitomo et al. nor Joo teach the claimed oxidizing conditions. The only teaching in Joo of oxidizing using thermal oxidation or plasma oxidation refers to the oxidation of the sides of ruthenium layer pattern 45a, which forms the lower electrode of Joo's capacitor. See col. 4, lines 47-50. Joo does not teach or suggest oxidizing a second layer of dielectric material.

V. Claims 11-12 and 62-63 are patentable over the combined teachings of Kunitomo et al., Joo, and Kingon et al.

The Examiner maintains that it would have been obvious to form a gas permeable electrode on an upper electrode as recited in claim 11, referring to Kingon et al., who teach a top electrode which may comprise a hybrid electrode structure such as Pt/RuO₂. The Examiner refers to the abstract of Kingon et al., asserting that one skilled in the art would have been motivated to form a gas permeable electrode on an upper electrode as claimed because Kingon et al. teach that the hybrid electrode structures improve capacitor performance. However, this teaching clearly refers to the benefits provided by the hybrid electrode structure (Pt/RuO₂) itself, not by the formation of a gas permeable electrode on an upper electrode.

Nor does Kingon et al. disclose oxidizing the upper layer electrode through a gas permeable electrode as claimed and as acknowledged by the Examiner at page 9 of the final rejection. The Examiner asserts that such would have been prima facie obvious in the absence of

new or unexpected results. However, applicants wish to point out that the examiner has the burden of establishing a *prima facie* case of obviousness. The Examiner has failed to present any facts or evidence, nor has she pointed to any reference, which suggests forming a gas permeable electrode on an upper layer electrode and oxidizing the upper layer electrode through the gas permeable electrode. Accordingly, applicants are under no obligation to provide evidence of unexpected results.

VI. Conclusion

The prior art references clearly do not anticipate, nor render obvious, the claims of the present invention as they do not teach or suggest a method of forming a capacitor in which a high dielectric constant oxide dielectric material is oxidized simultaneously with a conductive oxide electrode using a gas plasma treatment such that the surface of the conductive oxide electrode is provided with enough oxygen to provide stability with the first layer of high dielectric constant oxide dielectric material as claimed. The Board is requested to reverse the rejections of claims 1-6, 8-12, 15, 22-30, 37-50, 57-63, 74-76 and 100-105 in their entirety.

Respectfully submitted,

KILLWORTH, GOTTMAN, HAGAN
& SCHAEFF, LLP

By Susan M. Luna
Susan M. Luna
Registration No. 38,769

One Dayton Centre
One South Main Street, Suite 500
Dayton, Ohio 45402-2023
Telephone: 937/223-2050
Facsimile: 937/223-0724

SML/

APPENDIX

The Claims on Appeal

1. A method of forming a capacitor comprising providing a conductive oxide electrode, depositing a first layer of a high dielectric constant oxide dielectric material on said conductive oxide electrode, oxidizing said conductive oxide electrode and said first layer of said high dielectric constant oxide dielectric material under oxidizing conditions such that at least the surface of said conductive oxide electrode is provided with enough oxygen to provide stability with said first layer of high dielectric constant oxide dielectric material, depositing a second layer of said high dielectric constant oxide dielectric material on said first layer of said high dielectric constant oxide dielectric material, and depositing an upper layer electrode on said second layer of said high dielectric constant oxide dielectric material.
2. A method as claimed in claim 1 wherein said high dielectric constant oxide dielectric material is oxidized using a gas plasma.
3. A method as claimed in claim 2 wherein said gas plasma is formed from a gas selected from the group consisting of O₂ and O₃.
4. A method as claimed in claim 2 wherein the gas plasma oxidation is carried out at a temperature in the range of from about 250° to about 500°C.
5. A method as claimed in claim 1 wherein said high dielectric constant oxide dielectric material is Ta₂O₅.
6. A method as claimed in claim 5 wherein said high dielectric constant oxide dielectric material is amorphous Ta₂O₅.

8. A method of forming a capacitor comprising providing a conductive oxide electrode, depositing a first layer of a high dielectric constant oxide dielectric material on said conductive oxide electrode, oxidizing said conductive oxide electrode and said first layer of said high dielectric constant oxide dielectric material under oxidizing conditions, depositing a second layer of said high dielectric constant oxide dielectric material on said first layer of said high dielectric constant oxide dielectric material, depositing an upper layer electrode on said second layer of said high dielectric constant oxide dielectric material, and oxidizing said upper layer electrode under oxidizing conditions.

9. A method as claimed in claim 8 wherein said upper layer electrode is oxidized using a gas plasma.

10. A method as claimed in claim 9 wherein said gas plasma oxidation is carried out at a temperature in the range of from about 250° to about 500°C.

11. A method of forming a capacitor comprising providing a conductive oxide electrode, depositing a first layer of a high dielectric constant oxide dielectric material on said conductive oxide electrode, oxidizing said conductive oxide electrode and said first layer of said high dielectric constant oxide dielectric material under oxidizing conditions, depositing a second layer of said high dielectric constant oxide dielectric material on said first layer of said high dielectric constant oxide dielectric material, depositing an upper layer electrode on said second layer of said high dielectric constant oxide dielectric material, depositing a gas permeable electrode on said upper layer electrode, and oxidizing said upper layer electrode through said gas permeable electrode.

12. A method as claimed in claim 11 wherein said gas permeable electrode comprises platinum.
15. A method of forming a capacitor comprising providing a conductive oxide electrode, depositing a first layer of a high dielectric constant oxide dielectric material comprising Ta_2O_5 on the conductive oxide electrode, oxidizing said conductive oxide electrode and said first layer of said high dielectric constant oxide dielectric material under oxidizing conditions such that at least the surface of said conductive oxide electrode is provided with enough oxygen to provide stability with said first layer of high dielectric constant oxide dielectric material, depositing a second layer of said high dielectric constant oxide dielectric material on said first layer of said high dielectric constant oxide dielectric material, oxidizing said second layer of said high dielectric constant oxide dielectric material, and depositing an upper layer electrode on said second layer of said high dielectric constant oxide dielectric material.
22. A method as claimed in claim 15 wherein said second layer of said high dielectric constant oxide dielectric material is oxidized by rapid thermal oxidation.
23. A method as claimed in claim 22 wherein the rapid thermal oxidation is performed at a temperature of less than about $700^{\circ}C$.
24. A method as claimed in claim 22 wherein the oxidation is performed in the presence of a gas selected from the group consisting of O_2 and N_2O .
25. A method as claimed in claim 15 further comprising crystallizing said second layer of said high dielectric constant oxide dielectric material prior to depositing said upper electrode.
26. A method as claimed in claim 25 wherein said second layer of said high dielectric constant oxide dielectric material is crystallized by heating said high dielectric constant oxide dielectric material at a temperature greater than about $700^{\circ}C$ in an inert atmosphere.

27. A method as claimed in claim 25 wherein said second layer of said high dielectric constant oxide dielectric material is crystallized and oxidized by heating said high dielectric constant oxide dielectric material at a temperature greater than about 700°C in an atmosphere containing a gas selected from the group consisting of O₂ and N₂O.

28. A method of forming a capacitor comprising providing a conductive oxide electrode, depositing a first layer of a dielectric material comprising Ta₂O₅ on said conductive oxide electrode, treating said conductive oxide electrode and said dielectric material under oxidizing conditions such that both said conductive oxide electrode and dielectric material are oxidized and such that at least the surface area of said conductive oxide electrode is provided with enough oxygen to provide stability with said first layer of dielectric material, depositing a second layer of a dielectric material comprising Ta₂O₅ on said first layer of said dielectric material, oxidizing said second layer of said dielectric material, crystallizing said second layer of said dielectric material, and depositing an upper layer electrode on said second layer of said dielectric material.

29. A method as claimed in claim 28 wherein said second layer of said dielectric material is crystallized by heating at a temperature of greater than about 700°C in an inert atmosphere.

30. A method as claimed in claim 28 wherein said second layer of said dielectric material is crystallized and oxidized by heating at a temperature of greater than about 700°C in an atmosphere containing a gas selected from the group consisting of O₂ and N₂O.

37. A method as claimed in claim 28 wherein said second layer of said dielectric material is oxidized by rapid thermal oxidation.

38. A method as claimed in claim 37 wherein said rapid thermal oxidation is carried out at a temperature of less than about 700°C.

39. A method as claimed in claim 37 wherein said rapid thermal oxidation is carried out in an atmosphere containing a gas selected from the group consisting of O_2 and N_2O .
40. A method of forming a capacitor comprising providing a conductive oxide electrode selected from the group consisting of RuO_x and IrO_x , depositing a first layer of a dielectric material selected from the group consisting of Ta_2O_5 and $Ba_xSr_{(1-x)}TiO_3$ on said conductive oxide electrode, oxidizing said conductive oxide electrode and said first layer of said dielectric material with a gas plasma such that at least the surface area of said conductive oxide electrode is provided with enough oxygen to provide stability with said first layer of dielectric material, depositing a second layer of said dielectric material on said first layer of said dielectric material, depositing an upper layer electrode on said second layer of said dielectric material, and oxidizing said upper layer electrode.
41. A method as claimed in claim 40 wherein said conductive oxide electrode and said first layer of said dielectric material are oxidized using a gas selected from the group consisting of O_2 and O_3 .
42. A method as claimed in claim 40 wherein the oxidation is carried out at a temperature in the range of from about 250° to about $500^\circ C$.
43. A method as claimed in claim 40 wherein said upper layer electrode is oxidized using a second gas plasma in an oxidizing environment.
44. A method as claimed in claim 43 wherein the oxidation of said upper layer electrode is carried out at a temperature in the range of from about 250° to about $500^\circ C$.
45. A method as claimed in claim 40 wherein said upper layer electrode is selected from the group consisting of RuO_x and IrO_x .

46. A method as claimed in claim 40 wherein said conductive oxide electrode comprises RuO_x and said first layer of said dielectric material comprises Ta_2O_5 .

47. A method as claimed in claim 46 further comprising oxidizing the surface of said conductive oxide electrode prior to depositing said first layer of said dielectric material.

48. A method as claimed in claim 47 wherein the surface of said conductive oxide electrode is oxidized at a temperature in the range of from about 400° to about 475°C .

49. A method as claimed in claim 47 wherein the surface of said conductive oxide electrode is oxidized in an atmosphere containing a gas selected from the group consisting of O_2 , O_3 , and N_2O .

50. A method of forming a capacitor comprising providing a conductive oxide electrode selected from the group consisting of RuO_x and IrO_x , depositing a first layer of a dielectric material selected from the group consisting of Ta_2O_5 and $\text{Ba}_x\text{Sr}_{(1-x)}\text{TiO}_3$ on said conductive oxide electrode, oxidizing said conductive oxide electrode and said first layer of said dielectric material using a gas plasma under oxidizing conditions, depositing a second layer of said dielectric material on said first layer of said dielectric material, oxidizing said second layer of said dielectric material, depositing an upper layer electrode on said second layer of said dielectric material, and oxidizing said upper layer electrode.

57. A method as claimed in claim 50 wherein said second layer of said dielectric material is oxidized by rapid thermal oxidation.

58. A method as claimed in claim 57 wherein the oxidation is carried out at a temperature less than about 700°C .

59. A method as claimed in claim 57 wherein the oxidation is carried out in an atmosphere containing a gas selected from the group consisting of O_2 and N_2O .
60. A method as claimed in claim 50 wherein said upper layer electrode is oxidized using a gas plasma under oxidizing conditions.
61. A method as claimed in claim 60 wherein the oxidation is carried out at a temperature in the range of from about 250° to about $500^\circ C$.
62. A method as claimed in claim 50 further comprising depositing a gas permeable electrode on said upper layer electrode prior to oxidizing said upper layer electrode.
63. A method as claimed in claim 62 wherein said gas permeable electrode comprises platinum.
74. A method as claimed in claim 1 wherein said high dielectric constant oxide dielectric material is selected from the group consisting of Ta_2O_5 and $Ba_xSr_{(1-x)}TiO_3$.
75. A method as claimed in claim 1 wherein said conductive oxide electrode is selected from the group consisting of RuO_x and IrO_x .
76. A method as claimed in claim 1 wherein said upper layer electrode is selected from the group consisting of RuO_x and IrO_x .
100. A method of forming a DRAM cell comprising providing a conductive oxide electrode, depositing a first layer of a high dielectric constant oxide dielectric material on said conductive oxide electrode, oxidizing said conductive oxide electrode and said first layer of said high dielectric constant oxide dielectric material under oxidizing conditions such that at least the surface area of said conductive oxide electrode is provided with enough oxygen to provide

stability with said first layer of high dielectric constant oxide dielectric material, depositing a second layer of said high dielectric constant oxide dielectric material on said first layer of said high dielectric constant oxide dielectric material, depositing an upper layer electrode on said second layer of said high dielectric constant oxide dielectric material, providing a field effect transistor having a pair of source/drain regions, electrically connecting one of said source/drain regions with said conductive oxide electrode and electrically connecting the other of said source/drain regions with a bit line.

101. A method as claimed in claim 100 wherein said high dielectric constant oxide dielectric material is oxidized using a gas plasma.

102. A method as claimed in claim 101 wherein said gas plasma is formed from a gas selected from the group consisting of O_2 and O_3 .

103. A method as claimed in claim 101 wherein the gas plasma oxidation is carried out at a temperature in the range of from about 250° to about $500^\circ C$.

104. A method as claimed in claim 100 wherein said high dielectric constant oxide dielectric material is Ta_2O_5 .

105. A method as claimed in claim 104 wherein said high dielectric constant oxide dielectric material is amorphous Ta_2O_5 .